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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,647	09/30/2003	Kwang Su Choe	YOR920030293US1 (16818)	4796
7590 Steven Fischman, ESQ. Scully, Scott, Murphy and Presser 400 Garden City Plaza Garden City, NY 11530			EXAMINER PADGETT, MARIANNE L	
			ART UNIT 1792	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/674,647	<b>Applicant(s)</b> CHOE ET AL.	
	<b>Examiner</b> MARIANNE L. PADGETT	<b>Art Unit</b> 1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11/24/2008 & 12/31/2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11, 13 and 16-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11, 13 and 16-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

Art Unit: 1792

1. A **Request for Continued Examination** under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/31/2008 & 11/24/2008 have been entered.

It is noted that the advisory action of 12/4/2008 stated that the 11/24/2008 amendment appeared to remove 112, first & second paragraph rejections of sections 1 & 3 of the action mailed 10/1/08, however the latest amendment also introduces new 112, first & second problems, as discussed below.

2. As **previously discussed**, it remains relevant that the requirement in all independent claims concerning the region of vacancies or voids being porous **must** consider this with respect to what applicants mean by "**porous**", which is **further** limited by claim 7, where this **dependent** claim states "said porous region of vacancies or voids has a **porosity of about 0.01 % or greater**". Note this claim is consistent with the original specification [0013], which states "a large concentration (**on the order of about 0.01 % or greater**) of vacancies or voids. The terms '**vacancies**' and '**voids**' are **interchangeably** used in the present invention to did now at a porous Si region" (emphasis added), hence porous must be read in light of both the specification & dependent claim 7. Note as "on the order of about" might be considered to be make the defined range of the specification slightly broader than that of dependent claim 7, dependent claim 7 will not be considered to be not further limiting to the independent claim. For these reasons it was previously noted that rejections over Sadana et al. (5,930,643) or Norcott et al. (6,486,037 B2), were not removed as the processes therein were directed to creating vacancies, as an interstitial vacancies, although the disclosures did not discuss creating porosity.

While the examiner finds it doubtful that porosities as low as about 0.01 % (0.01 void volume/100 parts total volume) would be called porous by most people or one of ordinary skill of the art, that **as claimed** the porosity region of the independent claims may have a porosity of 0.01 % (i.e. a

Art Unit: 1792

density of 99.99 % of theoretical) or even lower porosity, since the dependent claim is required to further limit the independent claim, thus the independent claims porosity region necessarily includes **porosity** of <0.01 % (i.e. 0.009, or 0.001, etc.), as all greater porosities are encompassed by the necessarily narrower range of the dependent claim. Considering the claimed & defined values, plus the taught interchangeability of vacancies & voids in the specification for the present invention, the examiner must conclude that it is the intent of the application as filed to include substrates having vacancies, such as interstitial vacancies or defects, as being considered porous, thus upon reconsideration in light of the specification, the examiner cannot consider the amendment of the independent claims to include the description of "porous" inserted before "region of vacancies or voids" to make any difference in the scope of the claims.

The references of Ulyashin et al. (6,806,171 B1: col. 4, line 62-col. 5, line 67, especially lines 1-5 & 54-60 calling 1-10% low porosity); Balucani (2008/0012114 A1: [0103-104] defining needs for calculating porosity & considering relatively low porosity to be lower than 40 %) and Siuzdak et al. (6,288,390 B1: col. 11, line 4-col. 12, line 48 teaching a minimum porosity of 4 % for silicon to be porous) remain instructive for teaching what is commonly considered porous or low porosity, however as applicant has been their own lexicographer, for purposes of examination we must consider the values as defined by applicants' specification.

3. The **amendment filed 11/24/2008** (entered with RCE request of 12/31/2008) is **objected** to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce **New Matter** into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: see below discussion combined with 112, first rejection over claims, as the limitations of like scope were added to both specification & claims.

Applicant is required to cancel the new matter in the reply to this Office Action.

Art Unit: 1792

**Claims 1-11, 13 & 16-25** are rejected under 35 U.S.C. **112**, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The blanket implantation of oxygen ions to a uniform depth added in independent claims 1, 23 & 24, plus paragraph [0037] is considered to encompass some aspects of new matter, because while blanket implantation was previously considered (original claim 14), the phrase "uniform depth" was not in the original claims, nor found in the original specification's disclosure, nor was a definition of uniform depth. The hand drawn cross-sectional illustration of the layered substrata figure 2C, cannot be considered to provide details for enablement or support or definition for uniform thickness. Furthermore, in paragraph [0012] applicants have defined "uniform" for the entire specification to always mean "a buried oxide region having a continuous interface with a Si-containing over-layer as well as the underlying Si-containing substrate wherein the variation of thickness across the entire wafer is less than 30% of the total thickness of the buried oxide layer", thus prohibiting any clear meaning for "uniform" when used in combination with "depth" of oxygen ion implantation. Thus, the "uniform depth" amendments in the independent claims & paragraph [0037] are considered to encompass **New Matter**.

The amendment to paragraph [0048] of the specification raises the issue of whether or not this amendment broadens the scope of the original disclosure, thus introducing new matter, by broadening the disclosure of the embodiment from removing excess ion implanted dopants, to generic removal of excess dopant species that may be from any source. The **original** disclosure only discusses this embodiment with respect to excess ion implanted dopant & removing dopant ions, not generic dopant species, thus changing the disclosure to a broader scope of any dopant species, not necessarily ions & not necessarily from ion implantation, hence encompassing **New Matter**. While paragraph [0027] discusses generic doped substrates, with the option of creating doped substrates via ion implanting, there is no indication in

Art Unit: 1792

[0027] that the amount of dopant can be in excess or in need of altering. For these reasons, the amendment to [0048] & similar addition to the independent claims 1, 23 & 24, which do not require ion implantation to cause the doping of the silicon-containing substrate, must be considered to encompass **New Matter**, lacking any clear showing in the original specification that necessitates or indicates inclusion of broader sources of doping in this process. It is noted that except for the broader scope with respect doping in the claim limitations of "next annealing... hydrogen containing ambient to reduce the level of dopant...", [0048] supports this limitation, with sufficient discussion of H-ambient & the effect of reducing dopant levels, but only with respect to dopants that have been ion implanted in excess, where it doesn't support the ability to reduce dopant concentrations regardless of original concentrations, nor were sources other than ion implantation suggested, i.e. regardless of origin.

4. **Claims 1-11, 13 & 16-25** are rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Use relative terms that lack clear metes and bounds in the claims or in a clear definition in the specification or in cited relevant prior art, is vague and indefinite. In the independent claims, "uniform" in "uniform depth" lacks a clear scope of what is meant by uniform as a description of depth, since the phrase was not in the original specification, as a hand-drawn figure is not a showing of scope or definition of uniform, and as discussed above "uniform" was officially defined for the whole specification, regardless of what it modified, so as to create in unclear meaning in the claims for the newly amended use. Note with respect to that definition that the less than 30 % variation in the thickness of the [uniform] buried oxide layer region, as defined in [0012], can not be properly transferred to the newly claimed uniform depth of O-implantation, as there is no apparent evidence of any direct correspondence of the taught/defined variation on thickness & the newly claimed uniform depth of oxygen implantation. Also considering what may be meant by "uniform depth", it could mean all ions are implanted to be

Art Unit: 1792

approximately the same depth, or a range of depths is approximately the same where implantation occurs, etc., and further what scale uniform is to be considered on (microscopic, macroscopic, range of acceptable variation, etc.) is not known.

5. The following is a quotation of the appropriate paragraphs of **35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of **35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **1-11, 13 & 16-25** are rejected under 35 U.S.C. **102(e)** as being anticipated by or, in the alternative, under 35 U.S.C. **103(a)** as obvious over **Bendernagel et al. ((6,800,518 B2)**, which

Art Unit: 1792

incorporates PN **5,930,643 to Sadana et al.** by reference), as discussed in section 7 of the action mailed 6/14/2007.

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicants have not met the above stated criteria, nor have they presented any other sufficient arguments to overcome this rejection with respect to by **Bendernagel et al.** (6,800,518 B2), since they are supplied 131 affidavit was defective. See discussion in section 2 of the action mailed 4/8/2008.

With respect to new limitations added to the independent claims in the amendment of 11/24/2008, **Bendernagel et al.** (518), while teaching masking as one embodiment that may be employed with the ion implantation of oxygen, does not necessarily require that masking or patterning be employed, specifically noting in col. 9, lines 62-64, pointed out by applicants, that "... ion implantation process wherein ions are implanted only into **predetermined areas...**" (emphasis added), which encompasses selection of an entire surface area, selectively deposited to a desired depth, such as in Bendernagel et al.'s claim 14(c) "ions into predetermined areas...implant regions at or near said interface", which may be considered to read on possible meanings of uniform depth and doesn't necessitate patterning. Alternatively, if one considers predetermined area not to necessarily encompass blanket implantation, it must be further considered that it would have been obvious to one of ordinary skill in the art that discontinuous patterning versus blanket implantation is an obvious difference chosen dependent on particular enduse & circuit design, etc., having NO unexpected or unobvious significance in & of itself, with respect to processing techniques or procedures, especially noting that applicants' specification provides no special significance, as the options

Art Unit: 1792

are equivalently taught alternatives of blanket & pattern deposition in [0037], thus shows no unexpected results obtained for it either option of patterning or blanket deposition.

Also, it is noted that Bendernagel et al., in col. 9, lines 40-50, teach hydrogen annealing for the claimed purpose of lowering the level of dopants, where the hydrogen anneal is also after oxygen annealing, thus while this amendment to the hydrogen annealing fixes previous 112 issues, it is a limitation covered by this reference, thus provides no differentiation from the prior art.

As previously discussed applicants added a requirement for the **hydrogen ambient anneal after** formation of the silicon-on-insulator structure, however Bendernagel et al. (518) particularly teach such a step on col. 9, lines 40-50 sequential to the high-temperature oxidation anneal, teaching that "During the high-temperature annealing step, dopants present in substrate 10 may defuse from substrate 10 into the Si over-layer 30. If the level of doping concentration in Si over-layer 30 is too high, for a given device application, the structure shown in FIG. 1 may be subject to a post hydrogen annealing process. The post hydrogen anneal includes the same or different conditions as that of the optional hydrogen anneal mentioned above. A preferred post hydrogen anneal that may be employed in the present invention is a 0.25-3 hour anneal in low-pressure (82 Torr or less) hydrogen ambient at 1100-1150°C." Therefore, the new limitation added to the claims by applicants is clearly covered by the disclosure of Bendernagel et al.

With respect to previously discussed processing as a whole, Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & buried void plane structures, by forming a layer of porous silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current ( $\sim 0.1$ -20 mA/cm<sup>2</sup>) & voltage ( $\sim 0.1$ -10 volts typical,  $\sim 0.5$ -5 volts preferred) used, the HF concentration, and the dopant type & concentration in the wafer, and where thickness of the porous silicon layer may additionally depend on the time ( $\sim 30$  sec.-10 min.,  $\sim 1$ -5 min. more highly preferred) of anodization process. For this process

Art Unit: 1792

Bendernagel et al. teach that the "semiconductor **wafer needs to be doped**, preferably but not necessarily with **p-type** doping atoms. When a **boron**-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about  $1E15$  to about  $1E19$  atom/cm<sup>3</sup>..." (emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about  $1E16$ - $2E18$  atoms/cm<sup>2</sup>, implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm<sup>2</sup>, and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given ( $\sim 5E16$ - $2E17$  atoms/cm<sup>2</sup>,  $\sim 150$ -300 KeV,  $\sim 1.0$ -10 mA/cm<sup>2</sup>,  $\sim 550$ -600°C) as well as this high-temperature ion implantation step followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s) high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into buried void layers or buried conductive regions. The high-temperature annealing in is performed at temperatures of about 1300°C or greater, but less than the melting point of Si, which is 1415°C, and may be carried out in atmospheres of pure oxygen (O<sub>2</sub>), oxygen mixed with an inert gas or N<sub>2</sub>, or either without oxygen, or

Art Unit: 1792

vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a post hydrogen annealing process, which may use the same or different conditions (0.25-3 hours,  $\leq 82$  Torr H<sub>2</sub> ambient, T = 1100-1150°C) is then employed. Col. 9, lines 7-12 note that during annealing the porous silicon is consumed by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bendernagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be controlled by adjusting vertical depth of the porous silicon layer form during HF-anodization and the dose of the implanted ions. Particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 8 for doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically monocrystalline structure  $\equiv$  single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

With respect to applicants' claim 17, which is directed to specific parameters for a second oxygen implantation step, it is noted that Bendernagel et al.'s teachings on col. 8, lines 15-31 can be said to overlap with these parameters for their taught second implantation step at a normal room temperature, which is in the claimed temperature range for the second oxygen implantation, assuming that the other parameters employed for the second implantation can be any of the preceding taught parameters, which are overlapping with those claimed, or as suggested by Bendernagel et al. one may look at the exemplary art, such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via oxygen ion implantation, possibly through a capping layer, using a low-dose ion implantation ( $\sim \geq 5 \times 10^{16}$ ) at

Art Unit: 1792

high temperatures about  $\geq 200^{\circ}\text{C}$ , plus a second yet lower ion dose implantation at same or different energies carried out at cryogenic temperatures to about  $300^{\circ}\text{C}$  at doses of about  $2\text{E}14\text{-}4\text{E}15$  ion/ $\text{cm}^2$ . The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient ( $\text{N}_2$  or Ar) mixed with oxygen at temperatures from about  $1300^{\circ}\text{C}$  or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), thus providing specific parameters for the two-step oxygen ion implantation alternative, which read on claim parameters and which are employed with oxidation & annealing procedures as taught and claimed.

7. Given its relevance due to incorporation-by-reference, the previous discussion concerning **Sadana et al.** (643) is repeated below. Also discussion in section 2 above concerning porous & porosity as read in light of the specification, remains relevant, especially considering claim 7, such that the substrates' that have been treated to create vacancies must be considered inherently porous in light of applicants specification.

Applicants have previously argued (page 8 of 10/15/07 response) that oxygen ion implantation does not expressly or inherently caused voids in semiconductor substrates, but may provide amorphization, however given the definition of porous and applicants specification, as voids are claimed in the alternative with "vacancies" & taught in the specification to be equivalent, which one of ordinary skill in the art would clearly consider to be encompassed by the taught defects or damaged regions of Sadana et al. (643), as was previously discussed & not contradicted by the claim language as defined, and as vacancies are a type of defect or damage inherently caused by ion implantation, thus considered to be equivalent concepts or semantics differences.

As noted above & previously, Sadana et al. (643) has all the parameters to the claimed oxygen ion implanting & annealing steps, for producing buried oxide layers of thicknesses claimed. While Sadana et al. does not discuss providing a silicon-containing semiconductor material in the substrate that has a region with "vacancies or voids located therein" the initial ion implanting step which creates **defects**

Art Unit: 1792

**with inherently include defects that may be described as "vacancies"**, as created defects would have been expected to include displacements of atoms in the silicon-containing substrate, thus vacancies.

Further note that while Sadana et al. (643) most explicitly discuss a 2-step procedure, their teachings are inclusive of "this low temperature/low dose ion implantation step may be carried out in either a single step with a single temperature or multiple steps with multiple temperatures, which range from about cryogenic to about 300°C or less", such that the multistep ion implantation procedure described thereby reads on applicant's claimed process, even if one considers the "providing..." step necessarily separate from the step of "implanting...", as the multistep sequence to produce the low temperature low dose implantation, encompasses or overlaps with those sets of applicants' oxygen ion implantation parameters.

As previously discussed, claimed temperatures for two oxygen ion implantations relate to Sadana et al. (discussed above ), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (**buried damage region & adjacent amorphous** layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the **defect containing amorphous region** is believed to enhance oxygen diffusion into the silicon & combine with the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence noting claimed parameters & claimed multiple ion implantations as discussed in Sadana et al. for taught advantages in producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques. Also note that exemplary buried oxide region thicknesses via Sadana et al.'s process include 1000 Angstroms, i.e. 100 nm (example 1, specifically col. 7, lines 60-62), relate to claimed thicknesses for buried oxide layers in semiconductor substrate constructions.

Art Unit: 1792

8. **Other art** of interest previously cited included **Sato et al.** (5,854,123) who is also performing ion implantation processes in conjunction with making SOI structures, and discusses annealing under hydrogen atmosphere, however this is after ion implanting with hydrogen ions (e.g. Ex. 6, col. 28, etc), thus the hydrogen anneal is not performed in a sufficiently relevant context. Also remaining of interest are previously applied references: **Houston et al.** (2002/0086463 A1), **optionally** in view of Sadana et al. (5,930,643), or **Sadana et al.** (643) alone, or **over Norcott et al. ((6,486,037 B2)**, which is the child of Sadana et al. ( 643), whose rejections were removed by the addition of the post oxidation hydrogen annealing, since nothing in the procedures taught therein suggested a hydrogen anneal at that point (after formation of the SOI) in the procedure.

An **update search** of the prior art finds **Greene et al.** (7,479,437 B2), which while not prior art is of interest for teachings of forming porous silicon layers in doped silicon substrates in order to form buried oxide layers, and subsequent annealing steps applied thereafter, including hydrogen baking to remove excess p-type dopant.

9. Applicant's arguments filed 11/24/2008 (plus RCE request of 12/31/08) & discussed above have been fully considered but they are not persuasive.

10. **Any inquiry** concerning this communication or earlier communications from the examiner should be directed to **Marianne L. Padgett** whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 9:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available

Art Unit: 1792

through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/  
Primary Examiner, Art Unit 1792

MLP/dictation software

3/11-12/2009